IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

BALLY MANUFACTURING CORPORATION, Plaintiff, v. D. GOTTLIEB & CO. and WILLIAMS ELECTRONICS, INC., Defendants.	)	CIVIL ACTION NO. 78 C 2246

PLAINTIFF'S FIRST REQUEST FOR ADMISSION AND SECOND SET OF INTERROGATORIES TO DEFENDANT WILLIAMS (REQUEST NO. 1 AND INTERROGATORIES NOS. 3 AND 4)

Plaintiff, Bally Manufacturing Corporation, herewith serves the following request for admission and interrogatory upon the defendant, Williams Electronics, Inc., under Rules 33 and 36, F.R.C.P.

Request No. 1. With regard to the patent in suit and the materials supplied by Williams under the Stipulation filed February 16, 1979 disclosing an example of the construction of a "Disco Fever" pinball machine made and sold by defendant Williams since the patent in suit issued, admit or deny separately for each of the following parts (a) - (fff):

(a) Components shown in the CPU Board Logic Diagrams including IC's 1, 13, 16, 17, 19, 20, 21 and 22,

IC's 26 and 14 for "later games", and other related components correspond to the following claim element of Claim 1: "a processor having program means for programming the processor and memory means for storing signals".

(b) The ball corresponds to the following claim element of Claim 1: "a physical mass capable of motion".

(c) Components shown on page 36 (Disco Fever Manual) including the flipper assembly D-7060, components shown in the Solenoid Schematic Diagram including the flipper switches and flipper solenoids, and other related components correspond to the following claim element of Claim 1: "player-operated control means for affecting the motion of the physical means".

(d) Assemblies shown on page 36 (Disco Fever Manual) including those assemblies associated with ball responsive switches enumerated 9-29, 33-35 and 38-40 on page 19 (Disco Fever Manual), components shown in the Playfield Switch Wiring Diagram including the ball responsive switches enumerated 9-29, 33-35 and 38-40, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 11 and 15-18, components shown in the CPU Board Logic Diagrams including the address and data buses,

and other related components correspond to the following claim element of Claim 1: "a plurality of response means for detecting the mass, each response means having signaling means associated therewith and operatively connected to the processor for signaling the processor that the response means has detected the mass".

(e) Components shown in the Playfield Lamp Wiring Diagram including lamps enumerated 5-48, components shown in the Insert Board Diagram including the six digit displays for the scores of the four players, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 10 and transistors, Q's 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77, components shown in the CPU Board Logic Diagrams including IC's 6 and 18, components shown in the Master Display Schematic Diagram including IC's 4 and 9-13, and other related components correspond to the following claim element of Claim 1: "a plurality of display means for presenting information based upon the detection of the mass by the response means, each display means having a display activation means associated therewith and operatively connected to the processor for activating the display means in response to a signal from the processor".

(f) Components shown in the Playfield Switch Wiring Diagram including the diodes, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, components shown in the CPU Board Logic Diagrams including IC's 1, 6, 17, 18, 20, 21 and 22 and IC's 14 and 26 ("later games"), components shown in the Playfield Lamp Wiring Diagram including the diodes, and other related components correspond to the following claim element of Claim 1: "multiplexing means operatively connected to the processor for cyclicly and sequentially enabling each of the signaling means to signal the processor that its associated response means has detected the mass, and for cyclicly and sequentially enabling each of the display activation means to activate its associated display means".

(g) Components shown in the CPU Board Logic Diagram including IC's 1 and 18, the address and data buses, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, and other related components correspond to the following claim element of Claim 1: "said processor having means for storing the signals from the signaling means enabled by the multiplexing means into the memory means, for addressing the program means and the memory means, and

for signaling the display activation means enabled by the multiplexing means, in response to the program means and the memory means".

(h) Components shown in the Playfield Switch Wiring Diagram including the aforementioned ball responsive switches, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including the aforementioned IC's 15-18, and other related components connected as shown correspond to the following claim element of Claim 2: "[t]he apparatus of claim 1 wherein the signaling means associated with the respective response means are operatively connected as a plurality of sets of elements in a matrix".

(i) Components shown in the Playfield Switch Wiring Diagram including the aforementioned diodes, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including the IC 11 output lines PB0-PB7, and other related components correspond to the following claim element of Claim 2: "the multiplexing means having means for cyclicly and sequentially enabling each set of elements of the matrix".

(j) Components shown in the Playfield Lamp Wiring Diagram including the aforementioned lamps, components shown in

the Driver Board Logic Diagram (sheet 1 of 2) including the aforementioned transistors, components shown in the Insert Board Diagram including the aforementioned six digit displays, components shown in the Master Display Schematic Diagram including the aforementioned IC's 4 and 9-13, and other related components connected as shown correspond to the following claim element of Claim 3: "[t]he apparatus of claim 1 wherein the display activation means associated with the respective display means are operatively connected as a plurality of sets of elements in a matrix".

(k) Components shown in the Playfield Lamp Wiring Diagram including the aforementioned diodes, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including output lines PB0-PB7 of IC 10, components shown in the CPU Board Logic Diagrams including output lines 0-15 of IC 6 and other related components connected as shown correspond to the following claim element of Claim 3: "the multiplexing means having means for cyclicly and sequentially enabling each set of elements of the matrix".

(l) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including Darlington transistors, Q's 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72,

74 and 76, components shown in the Master Display Schematic Diagram including IC's 5 and 8, and other related components correspond to the following claim element of Claim 4: "[t]he apparatus of claim 3 further comprising a display drive circuit operatively connected to the processor having a plurality of outputs, each output being connected to a display activation means in each set of elements, for selectively driving the display activation means within the set of elements enabled by the multiplexing means, as determined by a signal from the processor".

(m) Components shown in the Driver Board Logic Diagram including IC 10, components shown in the CPU Board Logic Diagrams including IC 18, the address and data buses and other related components correspond to the following claim element of Claim 5: "[t]he apparatus of claim 4 wherein the processor further comprises an input and output circuit means operatively connected to a port of the processor and having a register for temporarily storing signals from the processor representative of the display drive outputs to be activated before transferring the signals to the display drive circuit".

(n) Components shown in the Driver Board Logic Diagram including IC 10 output lines PA0-PA7, components shown in the CPU Board Logic Diagrams including IC 18 output lines PB0-PB7 correspond to the following claim element of Claim 5: "means for transferring said signals to said display drive circuit".

(o) The display lamps and displayed digits do not appear to flicker when activated but instead appear to be continuously on when activated.

(p) Components shown in the CPU Board Logic Diagrams including IC 1 and lines connecting IC 18 to IC 1, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including lines connecting IC 10 to IC 1 of the CPU Board Logic Diagrams, and other related components correspond to the following claim element of Claim 11: "[t]he apparatus of claim 1 wherein the processor further includes synchronizing means for synchronizing the multiplexing means with the processor means for signaling the display activation means enabled by the multiplexing means".

(q) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including Q's 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74 and 76 correspond

to the following claim element of Claim 12: "[t]he apparatus of claim 11 wherein a display means comprises a lamp, said apparatus comprising a lamp drive circuit".

(r) The aforementioned components with respect to part 1(q) above, shown in the Driver Board Logic Diagram (sheet 1 of 2) further include IC's 13 and 14 and correspond to the following claim element of Claim 12: "said synchronizing means further comprising means for synchronizing the lamp drive circuit with the multiplexing means and the processor means for signaling the display activation means enabled by the multiplexing means".

(s) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 17 and 18, and other related components correspond to the following claim element of Claim 13: "[t]he apparatus of claim 1 wherein a signaling means of the response means comprises a voltage source".

(t) The ball responsive switches 9-29, 33-35 and 38-40 shown in the Playfield Switch Wiring Diagram correspond to the following claim element of Claim 13: "a switch operable by the response means".

(u) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 11, and other related components correspond to the following claim element of Claim 15: "[t]he apparatus of claim 1 wherein the processor further has an input and output circuit means operatively connected to a port of the processor and having a register for storing input signals from the signaling means before transferring the signals to the port of the processor".

(v) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 11, components shown in the CPU Board Logic Diagrams including IC 1, the address and data buses, and other related components correspond to the following claim element of Claim 15: "means for transferring said signals to said port".

(w) The ball corresponds to the following claim element of Claim 16: "[t]he apparatus of claim 1 wherein the physical mass comprises a ball".

(x) The playing field 14 shown on pages 3 and 36 (Disco Fever Manual) corresponds to the following claim element of Claim 16: "said apparatus further comprising a downwardly inclined playing field".

(y) The ball shooter 16 shown on page 3 and other related components correspond to the following claim element of Claim 16: "means for ejecting the ball to the upper end of the playing field whereby the ball may roll downwardly under the force of gravity across the playing field".

(z) Components shown in the Insert Board Diagram including the six digit displays for the four players' score, and other related components correspond to the following claim element of Claim 22: "[t]he apparatus of claim 1 wherein the detection of the physical mass by a response means is assigned a score and the plurality of display means includes multiple digit scoring means for displaying digits representing a player's score".

(aa) Components shown in the Insert Board Diagram including individual digit displays of the aforementioned six digit displays, and other related components correspond to the following claim element of Claim 23: "[t]he apparatus of claim 22 wherein the multiple digit scoring means comprises a plurality of single digit display means for displaying a digit of a player's score, each single digit display means being energized one digit at a time".

(bb) Components shown in the Insert Board Diagram including the individual digit displays of the aforementioned six digit displays, and other related components correspond to the following claim element of Claim 24: "[t]he apparatus of claim 23 wherein the single digit display means comprises a segmented digit display".

(cc) Components shown in the Master Display Schematic Diagram including IC 9 and IC 10, and other related components correspond to the following claim element of Claim 24: "the display activation means for each segmented digit display comprises a digit drive circuit having a plurality of inputs and outputs corresponding to the segments of the digits".

(dd) Components shown in the Master Display Schematic Diagram including IC's 5 and 8, and other related components correspond to the following claim element of Claim 25: "[t]he apparatus of claim 24 further comprising a segment drive circuit operatively connected to the processor for driving the inputs as determined by the processor of each of the digit drives when the digit drive is enabled by the multiplexing means".

(ee) Components shown in the CPU Board Logic Diagrams including IC 18, and other related components correspond to the following claim element of Claim 26: "[t]he apparatus of claim 25 wherein the processor further comprises an input and output circuit means operatively connected to the processor and having a register for temporarily storing the signals from the processor representative of the digit to be displayed before transferring the signals to the segment drive circuit".

(ff) Components shown in the CPU Board Logic Diagrams including IC 18 output lines PB0-PB7 correspond to the following claim element of Claim 26: "means to transfer said signals to said segment drive circuit".

(gg) Components shown in the Power Supply Schematic Diagram including the minus 100 VDC power supply, and other related components correspond to the following claim element of Claim 27: "[t]he apparatus of claim 1 wherein the display activation means associated with a display means comprises a power source".

(hh) Components shown in the Master Display Schematic Diagram including IC 9 and IC 10, and other related components correspond to the following claim element

of Claim 27: "a transistor switch means for operatively coupling the power source and the display means in response to the signal from the processor".

(ii) Components shown in the CPU Board Logic Diagrams including IC 6 and other related components correspond to the following claim element of Claim 27: "the multiplexing means comprising a decoder for completing the circuit of the power source, transistor switch means and the display means".

(jj) Components shown in the CPU Board Logic Diagrams including the IC 1 port labeled $\overline{IRQ}$, and other related components correspond to the following claim element of Claim 33: "[t]he apparatus of claim 1 wherein the processor further includes an interrupt input port".

(kk) Components shown in the CPU Board Logic Diagrams including IC 23 and other related components correspond to the following claim element of Claim 33: "said apparatus further comprising monitoring means for determining the status of a condition of the apparatus".

(ll) Components shown in the CPU Board Logic Diagrams including IC 23 and other related components correspond to the following claim element of Claim 33: "having signaling means operatively connected to the interrupt

port of the processor for signaling the processor with respect to the condition".

(mm) Components shown in the CPU Board Logic Diagrams including IC 1, and other related components correspond to the following claim element of Claim 39: "[t]he apparatus of claim 33 wherein the processor further includes interrupt means responsive to the signaling means supplied to the interrupt port for providing immediate processing of a condition determined by the monitoring means".

(nn) Components shown in the CPU Board Logic Diagrams including IC's 1, 13, 16, 17, 19, 20, 21 and 22, IC's 26 and 14 for "later games", and other related components correspond to the following claim element of Claim 45: "[a] pinball game comprising a processor having programming means and memory means".

(oo) The ball corresponds to the following claim element of Claim 45: "a ball".

(pp) The playfield 14 shown on pages 3 and 36 (Disco Fever Manual) corresponds to the following claim element of Claim 45: "a downwardly inclined playing field".

(qq) Components shown on page 3 (Disco Fever Manual) including the ball shooter, and other related components correspond to the following claim element of Claim 45: "player operated means for ejecting the ball on to the playing field whereby the ball may roll downwardly".

(rr) Assemblies shown on page 36 (Disco Fever Manual) including those assemblies associated with ball responsive switches enumerated 9-29, 33-35 and 38-40 on page 19 (Disco Fever Manual), components shown in the Playfield Switch Wiring Diagram including the ball responsive switches enumerated 9-29, 33-35 and 38-40, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 11 and 15-18, components shown on the CPU Board Logic Diagrams including the address and data buses, and other related components correspond to the following claim element of Claim 45: "a plurality of response means for detecting the ball and having signaling means associated therewith and operatively connected to the processor for signaling the processor that the response means has detected the ball".

(ss) Components shown in the Playfield Lamp Wiring Diagram including lamps enumerated 5-48, components shown in the Insert Board Diagram including the six digit displays for the scores of the four players, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 10 and transistors, Q's 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77, components shown in the CPU Board Logic Diagrams including IC's 6 and 18, components shown in the Master Display Schematic Diagram including IC's 4 and 9-13, and other related components correspond to the following claim element of Claim 45: "a plurality of display means for presenting information based upon the detection of the ball by the response means and having display activation means associated therewith and operatively connected to the processor for activating the display means in response to a signal from the processor".

(tt) Components shown in the Playfield Switch Wiring Diagram including the diodes, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, components shown in the CPU Board Logic Diagrams including IC's 1, 6, 17, 18, 20, 21 and 22 and IC's 14 and 26 ("later games"), and other related components

correspond to the following claim element of Claim 45: "multiplexing means operatively connected to the processor for cyclicly and sequentially enabling the signaling means to signal the processor that its associated response means has detected the ball, and for cyclicly and sequentially enabling the display activation means to activate its associated display means".

(uu) Components shown in the CPU Board Logic Diagrams including IC's 1 and 18, the address and data buses, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, and other related components correspond to the following claim element of Claim 45: "said processor having means for storing the signals from the signaling means enabled by the multiplexing means in the memory means, for addressing the program means and the memory means, and for signaling the display activation means enabled by the multiplexing means, in response to the program means and the memory means".

(vv) Components shown in the CPU Board Logic Diagrams including IC's 1, 13, 16, 17, 19, 20, 21 and 22, IC's 26 and 14 for "later games", and other related components

correspond to the following claim element of Claim 52: "[a] pinball game comprising a digital processor having programming means for programming the processor, and memory means for storing signals".

(ww) The ball corresponds to the following claim element of Claim 52: "a ball".

(xx) The playfield 14 shown on pages 3 and 36 (Disco Fever Manual) corresponds to the following claim element of Claim 52: "a downwardly inclined playing field".

(yy) Components shown on page 3 (Disco Fever Manual) including the ball shooter, and other related components correspond to the following claim element of Claim 52: "player operated means for ejecting the ball onto the playing field whereby the ball may roll downwardly".

(zz) Assemblies shown on page 36 (Disco Fever Manual) including those assemblies associated with ball responsive switches enumerated 9-29, 33-35 and 38-40 on page 19 (Disco Fever Manual), components shown in the Playfield Switch Wiring Diagram including the ball responsive switches enumerated 9-29, 33-35 and 38-40, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 11 and 15-18, components

shown in the CPU Board Logic Diagrams including the address and data buses, and other related components correspond to the following claim element of Claim 52: "a plurality of response means for detecting the ball and having signaling means associated therewith and operatively connected to the processor for signaling the processor that the response means has detected the ball".

(aaa) Components shown in the Playfield Lamp Wiring Diagram including lamps enumerated 5-48, components shown in the Insert Board Diagram including the six digit displays for the scores of the four players, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 10 and transistors, Q's 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77, components shown in the CPU Board Logic Diagrams including IC's 6 and 18, components shown in the Master Display Schematic Diagram including IC's 4 and 9-13, and other related components correspond to the following claim element of Claim 52: "a plurality of display means for presenting information based upon the detection of the ball by the response means and having display activation means associated therewith and operatively connected to the processor for activating the display

means in response to a signal from the processor".

(bbb) Components shown in the CPU Board Logic Diagrams including IC's 1 and 18, the address and data buses, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, and other related components correspond to the following claim element of Claim 52: "said processor having means for transferring the signals from the signaling means to the memory means, for addressing the program means and the memory means, and for signaling the display activation means in response to the program means and memory means".

(ccc) Components shown in the Playfield Switch Wiring Diagram including the diodes, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 10 and 11, components shown in the CPU Board Logic Diagrams including IC's 1, 6, 17, 18, 20, 21 and 22 and IC's 14 and 26 ("later games"), components shown in the Playfield Lamp Wiring Diagram including the diodes, and other related components correspond to the following claim element of Claim 52: "the display activation means associated with the respective display means and signaling means associated with the respective response

means defining a plurality of operable elements, the game further comprising multiplexing means for cyclicly enabling at least some of said elements to perform their associated functions".

(ddd) Components shown in the Playfield Switch Wiring Diagram including the aforementioned ball responsive switches, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including the aforementioned IC's 11 and 15-18, components shown in the CPU Board Logic Diagrams including the aforementioned address and data buses, and other related components correspond to the following claim element of Claim 53: "[t]he game of claim 52 wherein said elements comprise said signaling means".

(eee) Components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 10 and transistors, Q's 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77, components shown in the Playfield Lamp Wiring Diagram, including the aforementioned lamps, components shown in the Insert Board Diagram including the aforementioned six digit displays, components shown in the Master Displays Schematic Diagram including IC's 4 and 9-13, and other related components correspond to the following claim element of Claim 54: "[t]he game

of claim 52 wherein said elements comprise said display activation means".

(fff) Components shown in the Playfield Switch Wiring Diagram including the aforementioned ball responsive switches, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC's 11 and 15-18, components shown in the CPU Board Logic Diagrams including the address and data buses, components shown in the Driver Board Logic Diagram (sheet 1 of 2) including IC 10 and transistors, Q's 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75 and 77, components shown in the Playfield Lamp Wiring Diagram including the aforementioned lamps, components shown in the Insert Board Diagram including the aforementioned six digit displays, components shown in the Master Displays Schematic Diagram including IC's 4 and 9-13, and other related components correspond to the following claim element of Claim 55: "[t]he game of claim 52 wherein said elements comprise said signaling means and said display activation means".

INTERROGATORY NO. 3

If defendant's response to any of parts nos. 1(a) - 1(fff) herein is other than an unqualified affirmative response:

(a) State in detail and separately for each part in which an unqualified affirmative response was not given each and every reason defendant relies upon for failure to give each such unqualified affirmative response;

(b) Identify separately for each part in which an unqualified affirmative response was not given, by column and line number of U.S. Patent 4,093,232 and document, page and line number in the file history of U.S. patent application Serial No. 576,980, all of the material contained therein relied upon by defendant in support of the reasons stated by defendant in response to paragraph (a) of this interrogatory;

(c) Identify separately for each part in which an unqualified affirmative response was not given, each and every document not referred to in defendant's response to paragraph (b) of this interrogatory, and the material contained therein by page and line number, relied upon by defendant in support of the reasons stated by defendant in response to paragraph (a) of this interrogatory;

(d) If any reason stated by defendant in response to paragraph (a) of this interrogatory relates to an uncertainty of defendant concerning the definition of any term used in the request for admission, state in detail (i) the reason for defendant's uncertainty as to the definition of each such term, (ii) defendant's contention as to the definition of each such term, and (iii) supply the information requested in paragraphs (b) and (c) of this interrogatory with respect to each such contention.

INTERROGATORY NO. 4

(a) Identify each and every model of solid state electronic pinball machines which defendant Williams has manufactured and/or sold. Identify each model by model number, tradename, or other trade or catalog designation.

(b) State when (1) the manufacture of each model listed in the answer to Interrogatory No. 4(a) began and ended, and (2) the sales by Williams of each such model began and ended.

(c) With respect to each model listed in the answer to Interrogatory No. 4(a) made or sold as of June 6, 1978 and thereafter,

(1) state whether any of such models are alleged to not be covered by or within the scope of the language

of any of claims 1, 2, 3, 4, 5, 6, 8, 11, 12, 13, 15, 16, 22, 23, 24, 25, 26, 27, 33, 39, 45, 47, 52, 53, 54 and 55 of U. S. Patent No. 4,093,232, and

(2) identify the particular model or models, if any, which are alleged not to be covered or within the scope of any of said claims.

(d) If it is defendant's contention in its answer to Interrogatory No. 4(c) that certain of such models are not covered by or within the scope of any claim of said Patent No. 4,093,232, with respect to each of those certain models, state the specific language of each of the claims on which defendant's contention is based.

BALLY MANUFACTURING CORPORATION

By William Konrad
William K. Konrad
Attorney for Plaintiff

March 6, 1979

Chicago, Illinois